Design and Modeling of Seventh-Order Delta-Sigma Modulator

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ABSTRACT

This paper presents a seventh-order multi-bit delta-sigma modulator to achieve 30-bit resolution. The modulator topology considered cascade of resonator with multiple feedforward structure (CRFF). The modulator employed the 3-bit quantizer with eight different levels. The signal transfer function (STF) and noise transfer function (NTF) discussed. The NTF zeroes are optimized to maximum suppression of quantization noise. Due to the feedforward topology the STF of the CRFF structure shows peaking rather than flat low-pass response. It is observed the peak response in the STF for the case of CRFF is quite higher, as compared to the cascade of integrator with multiple feedforward topology. Also, the poles o the NTF lies insides the unit circle, while zeroes are spread on the DC in the unit circle for higher performance. It is also observed that the poles and zeroes lies inside the unit circle for the case of STF. The multi-bit quantizer causes the quantization step smaller. The out-of-band gain (OBG) of the modulator is adjusted to 2.5 for maximum signal to noise ratio (SNR). The input signal amplitude for the higher order modulator is 0.65-V. The modulator is modeled in MATLAB and performance is evaluated for maximum SNR of 184 dB for oversampling ratio of 128.

Keywords: Operational amplifier, Delta-Sigma Modulator, CRFF, Quantizer, OBG

1. INTRODUCTION

A delta-sigma modulator popular for digitization of analog signals. It implements embedded noise shaping to enhance the performance of the modulator. While oversampling control the bandwidth for target performance. The seventh order multi-bit modulator proposed for higher performance. The topology implements the CRFF with 3-bit quantizer. A high-resolution third-order single-bit delta-sigma modulator investigated for biosensing application. The modulator can achieve SNR of 119dB without thermal noise simulation. Wireless and implantable biomedical applications, such as ECG (electrocardiography) and neural implants, have found recent interest in the integrated circuits community, due to the opportunity for improved system integration, resulting in lower cost, area and battery life. Within these systems, the analog front end consists of a low-power preamplifier followed by an ADC. An ADC is designed for front-end of biosensor applications. The ADC have a 16-bit successive approximation register (SAR) analog-to-digital converter (ADC) with analog front-end and optical front-end circuit to detect biomedical signal for electroencephalography (EEG) applications. The proposed integrated design is 16-bit SAR ADC that achieves exceptional performance while consuming very low consumption and high dynamic range (DR) in parallel two pairs of 8-bit SAR ADC with SC low-pass filter. The dynamic comparator contains an asynchronous control sampling switches between high and low potential to internally proposed the timing source to optimizing dissipation of half

comparator and digital circuit [1]. Modern biosensors play a critical role in healthcare and have a quickly growing commercial market. Compared to traditional optical-based sensing, electrochemical biosensors are attractive due to superior performance in response time, cost, complexity and potential for miniaturization. To address the shortcomings of traditional benchtop electrochemical instruments, in recent years, many complementary metal oxide semiconductor (CMOS) instrumentation circuits have been reported for electrochemical biosensors. This work provides a review and analysis of CMOS electrochemical instrumentation circuits. First, important concepts in electrochemical sensing are presented from an instrumentation point of view. Then, electrochemical instrumentation circuits are organized into functional classes, and reported CMOS circuits are reviewed and analyzed to illuminate design options and performance tradeoffs [2]. A two-channel micro-power incremental ADC, designed for biosensor interface circuits, is reported. It uses a noise-coupled multi-bit delta-sigma loop, integrated with a novel digital decimation filter operating in near-threshold. It was realized in the IBM 90 nm CMOS technology. The fabricated 90 nm CMOS prototype device, for a 1 V_{pp} differential input range, experimentally shows a 74dB SNDR up to 2 kHz (1 kHz/channel) signal bandwidth. The total measured power consumption of the modulator is 13.5 µW [3]. This biosensor interface presents an ultra-low power incremental ADC for biosensor interface circuits. The ADC consists of a resettable second-order delta-sigma (Δ Σ) modulator core and a resettable decimation filter. Several techniques are adopted to minimize its power consumption. A feedforward path is introduced to the modulator core to relax the signal swing and linearity requirement of the integrators. A correlated-double-sampling (CDS) technique is applied to reject the offset and 1/f noise, thereby removing the integrator leakage and relaxing the gain requirement of the OTA. A simple double-tailed inverter-based fully differential OTA using a thick-oxide CMOS is proposed to operate in the subthreshold region to fulfill both an ultra-low power and a large output swing at 1.2 V supply. The signal addition before the comparator in the feedforward architecture is performed in the current domain instead of the voltage domain to minimize the capacitive load to the integrators. The capacitors used in this design are of customized metal-oxide-metal (MOM) type to reach the minimum capacitance set by the kT/C noise limit. Fabricated with a 1P6M 0.18 µm CMOS technology, the presented incremental ADC consumes 600 nW at 2 kS/s from a 1.2 V supply and achieves 68.3 dB signal to noise and distortion ratio (SNDR) at the Nyquist frequency and an FOM of 0.14 pJ/conversion step. The core area is 100×120 µm [4]. This paper presents a low-power all-MOS delta-sigma ADC specifically optimized for the potentiostatic biasing and amperometric read-out of electrochemical sensors. The proposed architecture reuses the dynamic properties of the sensor itself to implement a continuous-time mixed electrochemical delta-sigma modulator with minimalist analog circuits fully integrable in purely digital CMOS technologies. A 25-µW smart electrochemical sensor demonstrator integrated in low-cost 1M CMOS technology with Au post-processing is presented. Experimental results show electrical dynamic range values exceeding 10-bit, while electrochemical figures exhibit linearity levels close to

R2=0.999 combined with RSD<15% in terms of reproducibility. A comparative test with commercial potentiostat equipment is also included to qualify the performance of the proposed ADC[5].

This paper proposed a third-order single-bit cascade-of-multiple-feedback (CIFB) delta-sigma modulator Analog-to-Digital Converter (ADC) for electroencephalogram (EEG) used in wearable bio-signal sensing. The modulator can achieve more than 16-bit resolution for signal bandwidth of 100 Hz. Consider the higher stability, CIFB topology is considered for the modulator. The signal transfer function (STF) does not show peak at the low frequencies. The noise transfer function (NTF) shows ideal third-order noise shaping. To achieve the higher signal-to-noise ratio (SNR) the out-of-band-gain (OBG) of 2.5 adjusted even third-order loop filter. The modulator uses oversampling ration of 128 for the targeted signal bandwidth. The CIFB structure allow maximum stability due to three digital-to-Analog (DAC) implemented and considering the smaller full-scale of the modulator. Due to CIFB topology larger swing inside the loop filter, that demand higher DC gain operational amplifier for the integrator. The loop filter will process signal as well as quantization noise in the proposed modulator. The CIFB modulator with out-of-band gain (OBG) of 2 and without NTF zero optimization can achieve SNR of 71,97,119 with OSR of 32, 64, 128, respectively for limited full-scale input signal of 400 mV. Also, the operational amplifier in the loop filter is investigate for limited DC gain requirement. Finally, the modulator is simulated for non-idealities of thermal noise and flicker noise.

After the introduction, the second section discuss the design of the third-order modulator design with CIFB structure, while the third section describes the modeling and simulation of the modulator and explain the functionality of the integrator with non-idealities. Finally, the section four concludes the paper.

2. MODULATOR DESIGN

A third-order modulator is proposed for the biosensing application. Due to smaller full scale, higher order loop is stable. Also, the CIFB topology allows for maximum feedback DAC response with higher stability. Three integrators inside the loop filter with 1-bit quantizer. The complete modulator is modeled using MATLAB toolbox Delta-Sigma Toolbox [12]. The out-of-band-gain (OBG) of 2.5 adjusted to cater the higher performance of the modulator. Also, this ensure the higher stability of the modulator. The modulator with CIFB loop filter will process signal as well as quantization noise in the proposed modulator. The CIFB modulator with out-of-band gain (OBG) of 2 and without NTF zero optimization can achieve SNR of 71,97,119 with OSR of 32, 64, 128, respectively for limited full-scale input signal of 400 mV. Due to the low pass modulator, the STF of the modulator have low pass behavior. While the NTF have high pass response to shape more quantization noise at high frequency as shown in Figure. 1. The coefficients of the proposed third order CIFB modulator obtained from Delta-Sigma Toolbox. These coefficients represent the ratio of capacitors at the discrete time implementation of the modulator. Table-I shows the coefficient of the proposed modulator structure. The signal-transfer function (STF) and noise transfer function (NTF) of the modulator is shown in Figure 1. As it is shown from the Figure 1 clearly that the OBG of the CIFB modulator is 6. While STF of the modulator shows low-pass response to allow those signals, which are at low frequencies and attenuate high frequency signal. The Figure 2 shows the output power spectral density (PSD) plot with SNR of 119, achieving effective number of bit (ENOB) of 19-bit. The modulator NTF shows a sharp noise shaping response due to the reason that

Table I : CIFB Cofficients

Parameters	Values
b_1	0.29
b_2	1.15
b_3	1.7
b_1	1
a_1	0.29
a_2	1.15
a_3	1.7
c_1	1
c_2	1
c_3	1

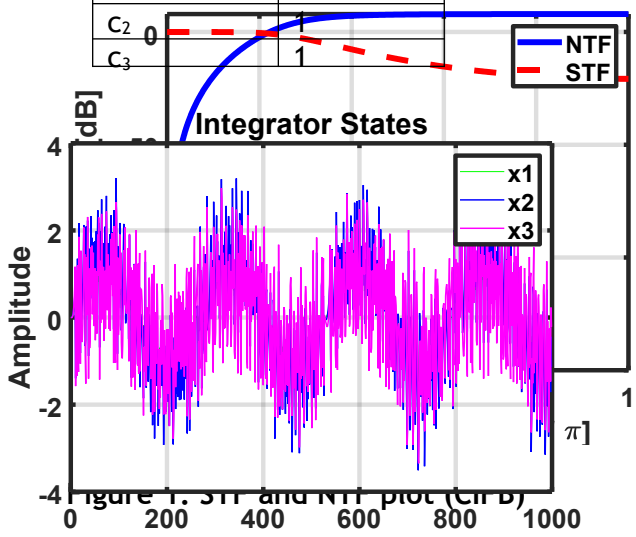

Figure 2: STF and NTF plot (CIFB)

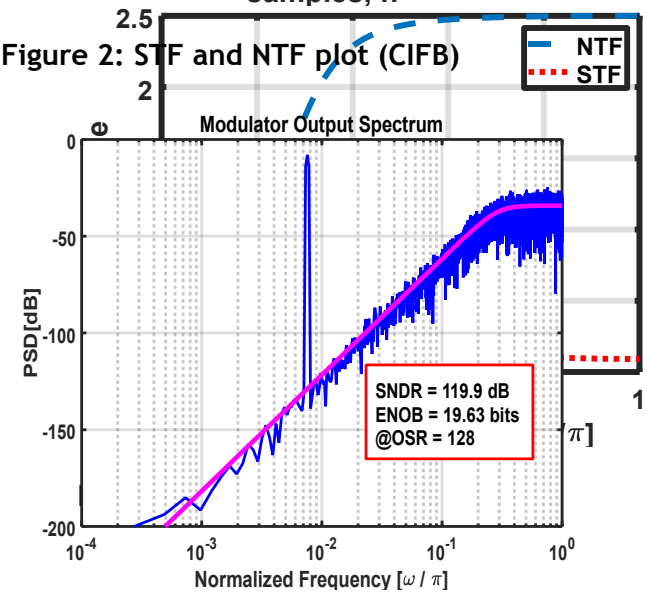

Figure 3: Output PSD plot (CIFB)

all integrator inside the loopfilter is assumed having infinite DC gain. Due to large OSR of 128, the signal bandwidth is small. Due to CIFB topology of the modulator the signal swing inside the loopfilter is large as a results operational amplifier with very high DC gain will be demanded for the suppression of the quantization noise. Due to CIFB topology the stability of the loopfilter is very high due to the advantage of multiple feedbacks, while the overall modulator becomes power hungry with many high DC gain amplifier inside the loopfilter.

1. RESULTS & DICUSSION

The third-order single-bit modulator simulated and modeled in MATLAB for biosensing application can achieve SNR of 119 dB with very small full-scale of 400 mV. The proposed modulator further simulated with circuit non-idealities using SDToolbox[13]. The modulator also investigated for circuit non-idealities like thermal noise and flicker noise.

4. CONCLUSION

A seventh-order multi-bit delta-sigma modulator to achieve 30-bit resolution. The modulator topology considered cascade of resonator with multiple feedforward structure (CRFF). The modulator employed the 3-bit quantizer with eight different levels. The signal transfer function (STF) and noise transfer function (NTF) discussed. The NTF zeroes are optimized to maximum suppression of quantization noise. Due to the feedforward topology the STF of the CRFF structure shows peaking rather than flat low-pass response. It is observed the peak response in the STF for the case of CRFF is quite higher, as compared to the cascade of integrator with multiple feedforward topology. Also, the poles o the NTF lies insides the unit circle, while zeroes are spread on the DC in the unit circle for higher performance. It is also observed that the poles and zeroes lies inside the unit circle for the case of STF. The multi-bit quantizer causes the quantization step smaller. The out-of-band gain (OBG) of the modulator is adjusted to 2.5 for maximum signal to noise ratio (SNR). The input signal amplitude for the higher order modulator is 0.65-V. The modulator is modeled in MATLAB and performance is evaluated for maximum SNR of 184 dB for oversampling ratio of 128.

5. ACKNOWLEDGMENT

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